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The Compact Muon Solenoid Experiment

CMS Note

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Trigger Studies for the CSC Muon System

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Abstract

The performance of the Compact Muon Solenoid (CMS) cathode strip chamber (CSC) trigger electronics was tested in the summer of 2003 in a test beam at CERN. A novel feature of the muon and pion beams was a 25 ns bunch structure similar to that of the LHC. Two CSCs were equipped with production on-chamber electronics and connected to near-final prototype off-chamber electronics. Both inputs and outputs of the CSC trigger electronics were recorded. The trigger algorithms were checked by a bit-for-bit comparison between the output trigger data and a detailed simulation of the trigger electronics run on the input trigger bits. The CSC trigger efficiency and position were studied under various conditions of CSC chamber high voltage, raw hit thresholds, particle rates, and chamber angles. These studies show that the design of the system is sound and will yield efficient muon triggering in CMS operation at the Large Hadron Collider.

1 Introduction

The endcap muon system of CMS contains 468 cathode-strip (CSC) chambers. The general plans for reading out and triggering with this system have been previously described [1, 2]. Prototypes of on-chamber electronics for this system were previously studied extensively [3, 4] in preparation for their mass-production. The CSC on-chamber electronics production is now complete, and these electronics have now been installed on the CSC chambers. However, the performance of the associated off-chamber electronics needs to be extensively checked as well before their mass production begins. In particular, most of the off-chamber electronics are housed in 60 VME 9U-size "peripheral" crates that are mounted around the periphery of the endcap muon iron disks. During the summer of 2003, a CERN test beam with LHC-like time structure was used to test this electronics system including near-final prototypes of all of the peripheral crate electronics. Key goals for this test beam were to demonstrate that the CSC on-chamber and peripheral crate electronics:

1. Work well together and with the CSC chambers as a system.
2. Trigger on muons with high efficiency and good position resolution.
3. Correctly identify the LHC bunch crossing with high probability.
4. Can handle the maximum particle rates expected at LHC.

This note describes the results of those beam tests.

A schematic of the CSC on-chamber and peripheral crate electronics system is shown below in Figure 1. For each CSC chamber, the on-chamber electronics is connected to one pair of boards in a peripheral crate: a Trigger MotherBoard (TMB) module and a Data acquisition MotherBoard (DMB) module. Each crate services one trigger sector, i.e. 60^o in muon stations 2-4 and 30^o in muon station 1. There are 9 TMB/DMB board pairs serving 9 CSC chambers in each crate. Trigger data from each sector is collected by the Muon Port Card (MPC) and sent by optical fiber to the CSC track finder. Most of the work during the summer 2003 test beam studies focused on the DMB and TMB modules and their associated on-chamber electronics.

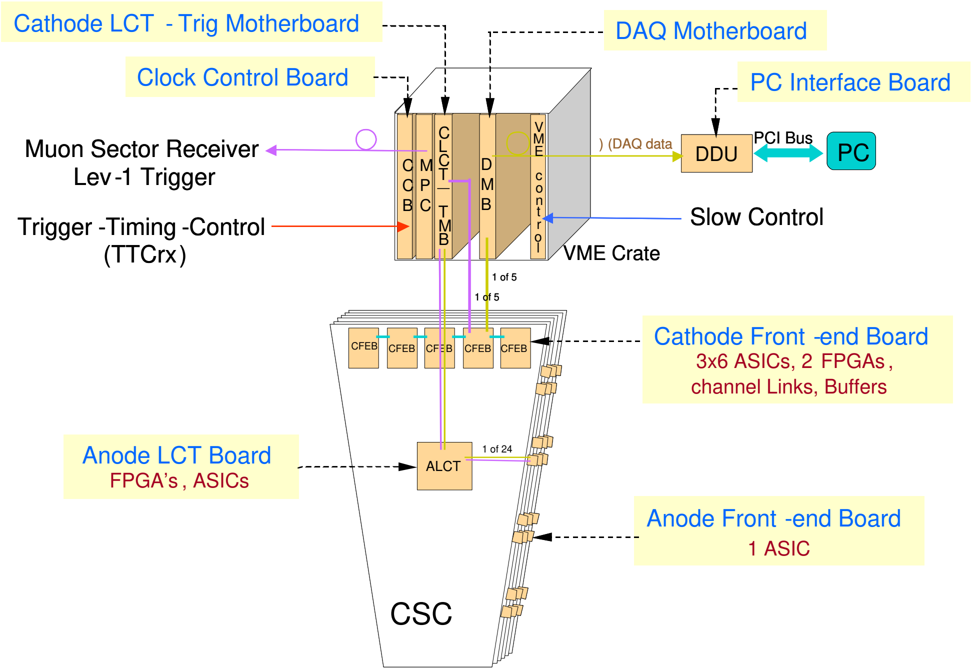

Figure 1: A block diagram of the electronics associated with each CSC muon chamber of CMS. There are 9 TMB/DMB board pairs per crate (not shown).

A short explanation of the function of each of the modules that are 1shown in Figure 1 and that were used in the test beam studies follows:

- CFEB [1, 5, 6] (Cathode Front-End Board): Contains sensitive amplifiers for cathode strip signals and creates parallel data and trigger data paths. The rise time of the cathode amplifiers is about 125 ns, and the fall time is about 250 ns. In the precision data path, analog charge information is stored in a switched capacitor array and subsequently digitized for readout upon receipt of a Level-1 trigger accept (L1A) signal. The digitized charge data are then sent to the DMB. For the trigger data path, custom comparator ASICs[1)] find the muon position on each CSC layer to a precision of one half-strip by comparing cathode signals on adjacent strips [7]. If a strip signal exceeds a programmable threshold, after a delay for signal peaking, that signal is compared to neighboring strips. If the signal is larger than both neighbors, it is determined to be the central strip in a cluster, and whether the track passed to the left or the right of the center of that strip is determined by comparing the signals adjacent strips on left and right. The half-strip bits are then sent to the TMB board. Each CFEB is attached to 96 cathode strips. There are 3, 4, or 5 CFEBs per CSC chamber, depending on the type of chamber.

- AFEB [8] (Anode Front-End Board): Contains a single 16-channel amplifier plus constant-fraction discriminator ASIC to digitize anode information. The hits are sent to the ALCT board. There are up to 42 AFEBs per CSC chamber.
- ALCT [2] (Anode Local Charged Track): There is one ALCT on each CSC chamber. For the trigger, this module finds patterns among the six layers of anode hits that look like a muon stub, and not background neutron-induced or other types of hits. It also time-aligns the anode hit information with the LHC clock, and determines the muon bunch crossing using a multiple-layer coincidence timing technique. Position and timing information for up to two anode LCT hit patterns (also called ALCTs) are sent to the TMB. For the data readout, the anode hits and the trigger hit patterns found are sent upon receipt of a level 1 trigger decision (L1A) to the TMB.
- TMB [2] (Trigger Mother Board): For the trigger, the TMB finds up to two cathode patterns, then requires a time coincidence between anode and cathode patterns. If a coincidence is found TMB combines the trigger information and sends the best two LCTs to the MPC using the more precise anode bunch crossing time. For the data readout, the TMB passes the anode ALCT information directly to the DMB, and sends in parallel the cathode comparator hits, cathode trigger patterns, and anode-cathode coincidence information to the DMB.
- MPC[2] (Muon Port Card): Collects LCTs from each of up to nine TMBs in a trigger sector and chooses the best three based on the muon stub quality. Sends this information to the CSC track finder system (Sector Processor, Sector Receiver).
- CCB[9] (Clock and Control Board): Provides the interface of the CSC system with the CMS Trigger, Timing and Control (TTC) system [10]. Distributes necessary signals for synchronized operation of a peripheral crate.
- DMB [1] (Data acquisition Mother Board): Upon arrival of L1A, collects data from ALCT, TMB and CFEBs, containing ALCTs, CLCTs and analog cathode information from a single CSC. Sends this event information to the DDU.
- DDU[1] (Detector-Dependant Unit): Upon arrival of L1A, collects data from all DMBs in a CSC sector and sends the information through the global DAQ path. In the version present at the test beam, this module was read out via Gigabit Ethernet to a PCI card and from there to disk on a Linux computer.

2 ALCT, CLCT, and TMB Trigger Algorithms

2.1 ALCT Algorithm

As previously mentioned, the ALCT finds patterns among the six layers of anode hits that look like a muon stub, and not background neutron-induced or other types of hits. It also time-aligns the anode hit information with the LHC clock, and determines the muon bunch crossing using a multiple-layer coincidence timing technique. Position and timing information for up to two anode LCT hit patterns (also called ALCTs) are sent to the TMB.

***Show or describe the ALCT envelope for collision and accelerator muon patterns.

***Was just copied from general description. Need to add details.

[1)] Application-Specific Integrated Circuit

2.2 CLCT Algorithm

As previously mentioned, the CLCT part of the TMB finds up to two cathode patterns among the six layers of cathode half-strip hits.

***Show or describe the CLCT envelope for muon patterns.

Relevant text from Jonathan:

- Fire 1/2-strip digital one-shots for 6 clock cycles.
- Construct di-strip hits from stagger-corrected 1/2-strips.
- Count 1/2-strip hits within pattern envelope for 160 key 1/2-strips.
- Count di-strip hits within pattern envelope for 40 key di-strips.
- Pre-trigger if any 1 of 160 1/2-strip envelopes or any 1 of 40 di-strip envelopes are over threshold.
- Select 1/2-strip envelopes: on each 1 of 5 CFEBs, find 1 of 32 key 1/2-strips with the highest number of hits within the corresponding envelope. If two or more keys have an equal number of hits, the lower number key is taken. This is done independantly for each CFEB, so that up to 5 low-Pt CLCTs may be found for the CSC chamber.
- Select di-strip envelopes likewise.
- Select 1/2-strips versus di-strips: On each 1 of 5 CFEBs, select between best 1/2-strip CLCT and best DiStrip CLCT. Take 1/2-strip CLCT if number of hits is above half-strip threshold, otherwise take Di-strip CLCT. Results in 0 to 5 CLCTs for the CSC, may be a mix of 1/2-strip and di-strip CLCTs.
- Remove duplicate CLCTs at CFEB boundaries: If CLCT for a particular CFEB has key 1/2-strip within the last 4 out of 32, and the CLCT on the next CFEB has key 1/2-strip within the first 4 out of 32, then the CLCT candidate on the next CFEB is deleted unless it has a higher number of hits, in which case the first CLCT is deleted.
- Select best 2 of 5 CLCTs by number of layers found within the envelope of hits. In the case of equal numbers of layers, priority is given to the CLCTs from the lowest-numbered CFEB.
- Pattern look-up: for the two selected CLCTs, compare the pattern of hits within the envelope to 7 pre-defined patterns. The match with the greatest number of hits is chosen. In case two patterns match an equal number of hits, then priority is given to the higher pattern number.

  *** Need to check this, also show a plot of the patterns or describe them in words.
- Swap CLCT order if the pattern number for the previously 2nd-best CLCT is higher than for the best, and also the best CLCT candidate is of the di-strip variety.
- Assign the final CLCT parameters (pattern number, position) after waiting for straggling hits by a delay which can be adjusted from 0 to 5 ***check this*** clocks.

***Need to fix the english and make it more understandable.

2.3 ALCT-CLCT Match Algorithm

The TMB matches the cathode patterns to the anode patterns by requiring a coincidence within a pre-defined time window. If a coincidence is found TMB combines the trigger information and sends the best two LCTs to the MPC using the more precise anode bunch crossing time.

***Was just copied from general description. Need to add details.

3 Test Beam Setup

3.1 Data-taking Conditions

The CSC setup was placed in the X5A test beam, which is a tertiary beam from CERN's SPS (400 GeV/c), providing a muon or pion beam of energy between 5 and 250 GeV. Collimators in the beam line allowed for control of the rate of particles. An important feature of the muon and pion beams during part of the running time was a 25 ns bunch structure similar to that of the LHC. and 48 bunches were filled out of the SPS total of 924 (the LHC has 3564 bunches). Within each bunch, particles arrived during a window 2.3 ns wide. Particles were extracted during a 1.5-2.5 s spill out of a 16.8 s ramp cycle. Muon rates up to $\approx 10^4$ per spill and pion rates up to $\approx 10^6$ per spill were available.

Pions at 150 GeV. Pion rates 10^4 to 10^6 per spill (?). Muons spectrum? Muon rate 10^3 to 5×10^3 per spill (?). Beam horizontal. Chambers set up with HV from Bertan power supplies, LV supplied to on-chamber electronics, cabling from chamber to peripheral crate electronics just as in the CMS setup.

***What else to say? Information from CERN web page.

3.2 X5A Setup

Two CSCs were equipped with production on-chamber electronics and connected to near-final prototype off-chamber electronics The test beam setup is shown in Figure 2. The two CSCs were placed about a meter apart and nominally rotated $20\,\deg$ with respect to the perpendicular to the beam axis, and vertically oriented, so that the beam represented an LHC muon at $20\,\deg$ polar angle and infinite momentum. All parts of the diagram shown in Figure 1 were implemented, including the Muon Port Card (MPC) that collects trigger information about muon segments from all of the TMB modules in a peripheral crate. The trigger electronics was set to form triggers from internal chamber information, but the readout was initiated by a three-fold coincidence of signals from the scintillator paddles of the beam hodoscope. The size of these paddles was approximately 10 cm on each side, well-matched to the size of the beam. The background rate of non-particle coincidences from this hodoscope was so low as to be unmeasured. The operation of the trigger electronics is checked by study of the data read out. A data block was created for every scintillator hodoscope coincidence. In cases where no CSC information was available, a short header was read out in order to obtain true efficiency measurements.

CSC event data is organized into three sub-categories: trigger anode data, trigger cathode plus anode/cathode time-coincidence data, and cathode precision charge-readout data. For each type of data, a time history of all channels is recorded.

For anode data, the raw data hits are recorded every 25 ns clock cycle for 16 time bins starting approximately 2 clocks before the typical muon arrival time. Anode hits for a typical event are shown in Figure 3 for each chamber layer. It can be seen that some hits are latched on successive clocks. This happens because in order to be absolutely sure to latch the data, the discriminator outputs have been designed to last longer than the time between clock cycles, typically 30-35 ns.

For cathode data, due to the relatively slow 100 ns rise time of the amplifiers, the precision charge measurements are recorded only every two clocks (50 ns). Either 8 or 16 time bins of precision charge measurement can be selected, starting approximately 250 ns before the peak charge is recorded. Projections of the cathode data versus position and time are shown for each of the CSC chamber layers in Figure 4. In the charge versus position projections (left side), the largest charge recorded on each strip is plotted. In the charge versus time projections (right side), the largest charge recorded for each time bin is plotted. One sees the typical 100 ns rise time and slightly longer fall time of the sensitive front-end strip amplifiers. Also shown on these plots are half-strip trigger hits. Cathode trigger hits are determined for the center of each cluster to a precision of one half-strip by a 16-channel 'Comparator' ASIC that compares the voltage level out of the cathode amplifier to a minimum threshold, and also compares the voltage levels on adjacent strips. The cathode trigger hits are recorded every 25 ns clock cycle in 7 time bins beginning approximately 2 samples (50 ns) before the peak charge.

An event display for both cathode and anode hits is shown in Figure 5. The cathode and anode trigger data is shown as individual hits at the time at which the signals exceeded threshold. In the cathode display, the maximum cathode charge is shown for each strip in red, the comparator $1/2$-strip bits are shown in blue, and the position of the trigger pattern (defined at layer 3) is shown in yellow.

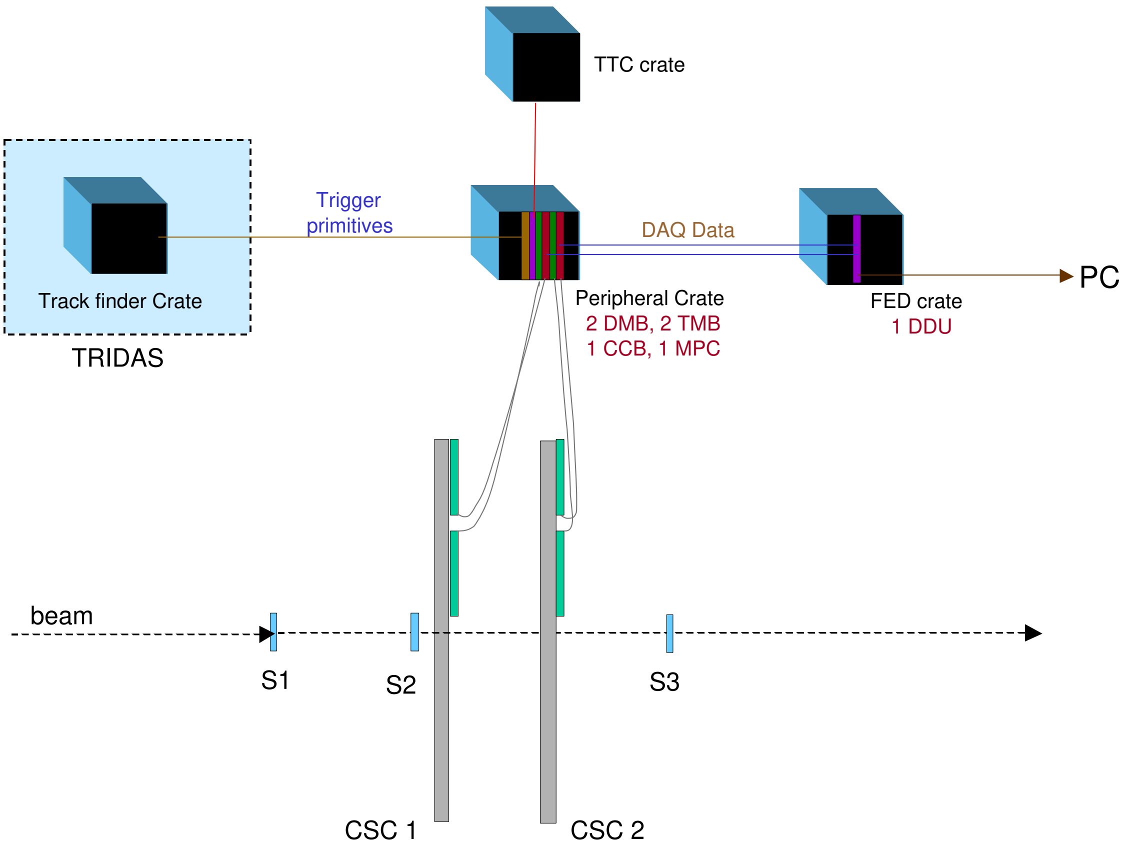

Figure 2: The summer 2003 CSC test beam setup. The beam line is vertical and passes through two CSC chambers that are mounted on the left (one is hidden behind the other). Blue cables run along the top from the on-chamber electronics to the right side where the peripheral crate electronics is located in a 9U-height VME crate. The peripheral crate electronics is then read out through an optical fiber to a PCI card, and thence to disk in the data acquisition computer in the control room.

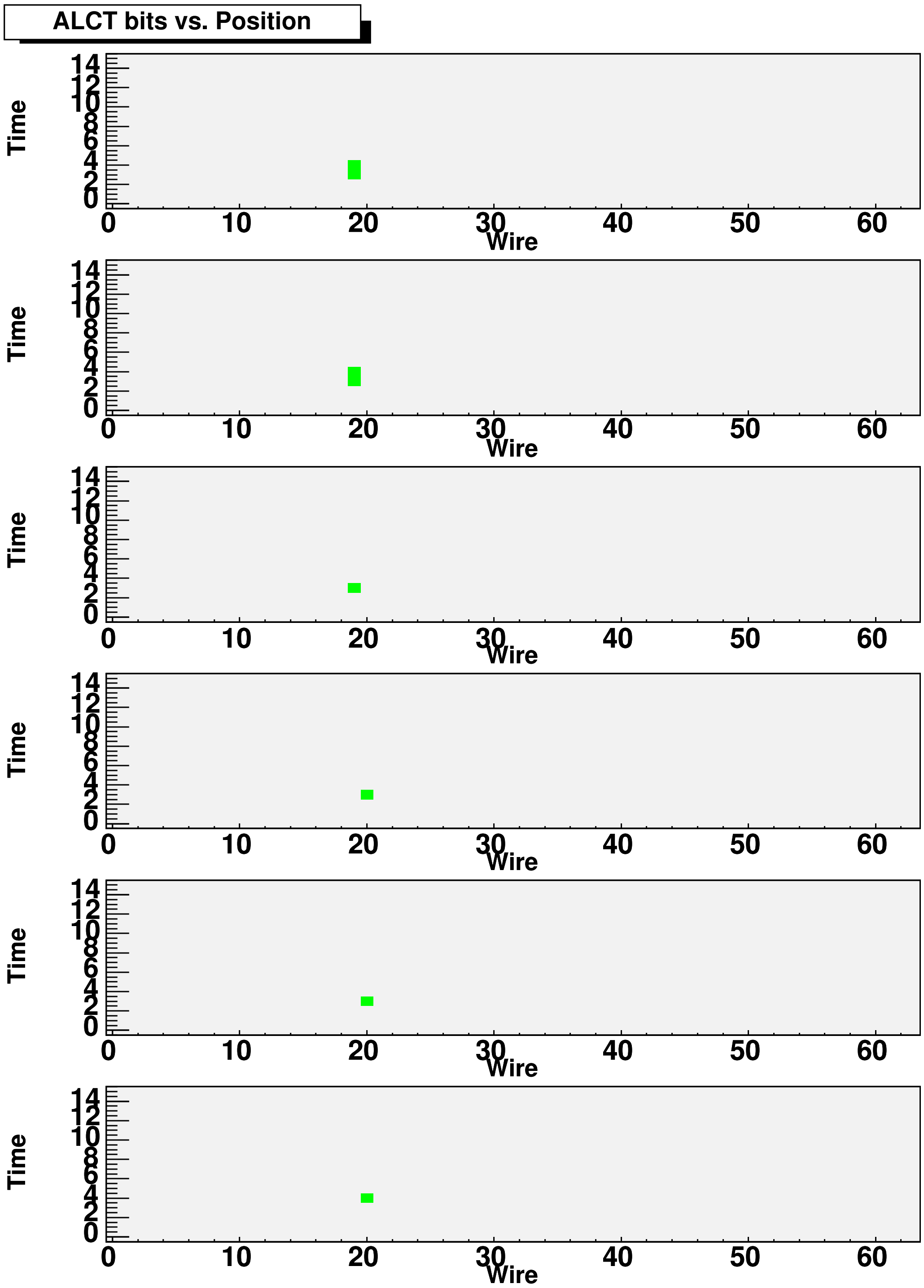

Figure 3: An event display showing the anode hits versus time and wire number for each chamber layer.

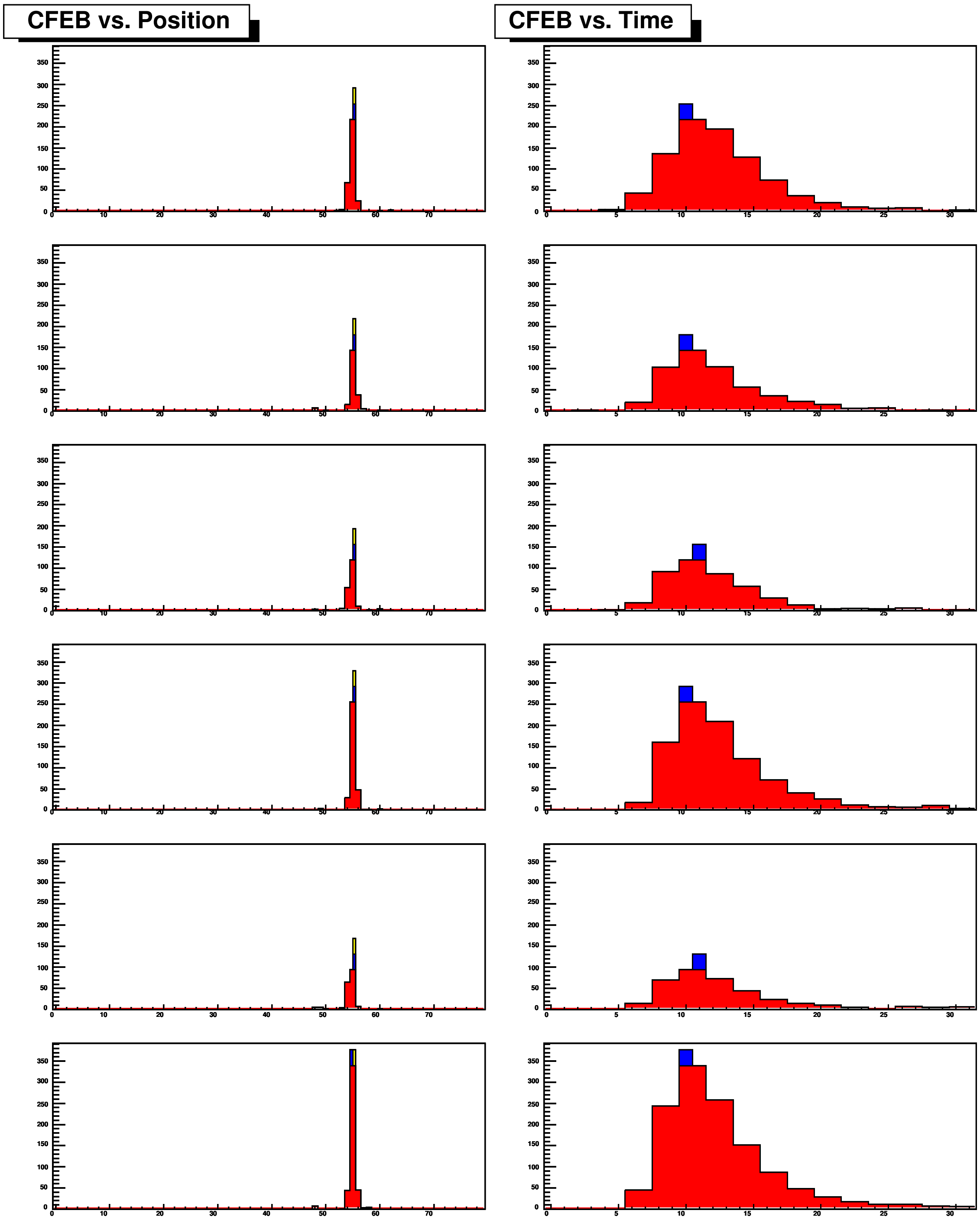

Figure 4: An event display showing profiles of the cathode hit data versus strip number (left) and time bin (right).

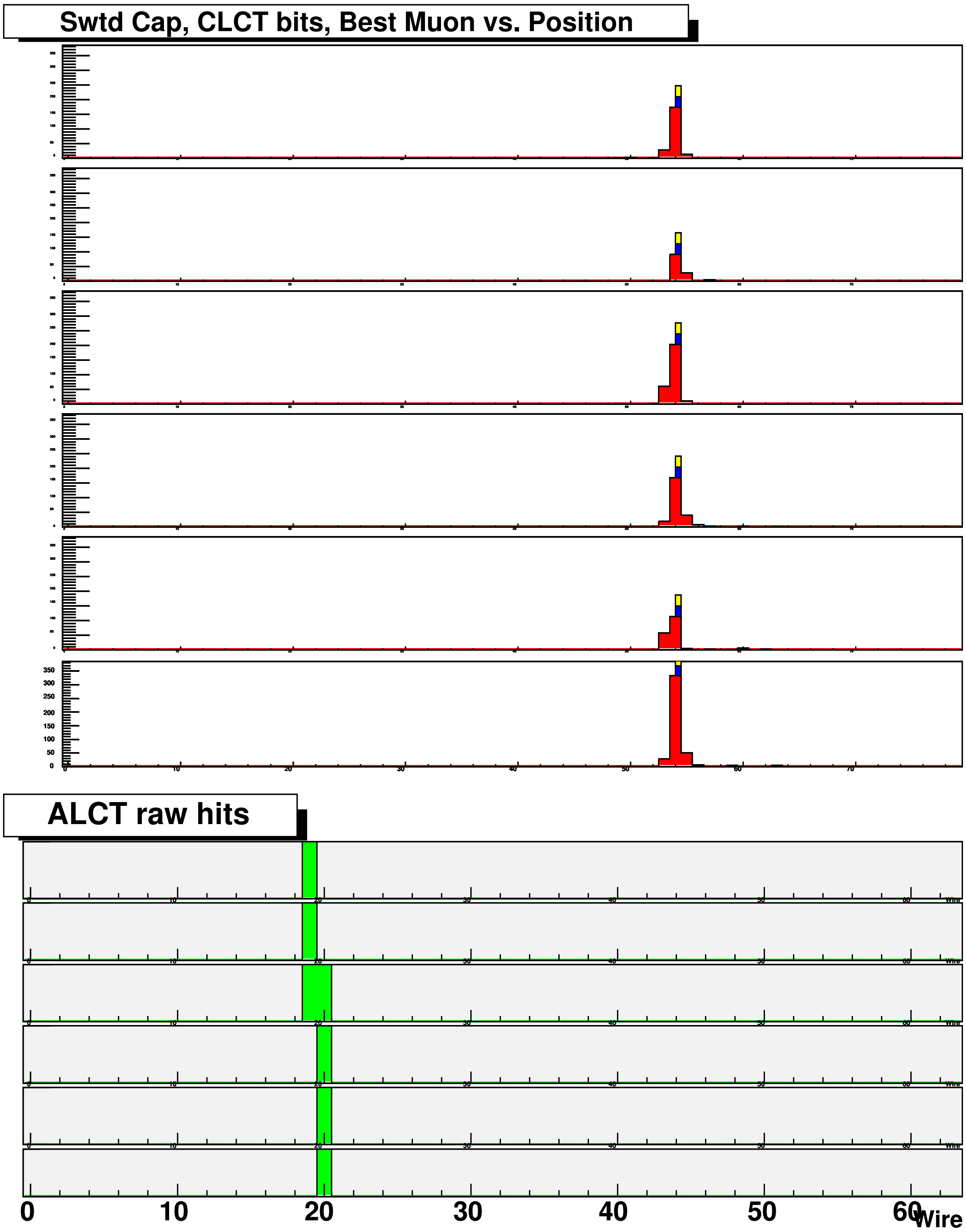

Figure 5: An event display showing the maximum cathode charge recorded on each strip (top) and the anode wires that recorded hits (bottom). The six layers of the CSC chambers are shown.

4 Trigger Setup and Timing

The first step in taking data is to time in the electronics system. A number of times need adjustment (this can be done either with cosmic ray hodoscope or test beam hodoscope triggers):

- CFEB readout timing: a CLCT data-available signal from the TMB is sent through the DMB to the CFEBs. This signal freezes data in the CFEB switched capacitor arrays until a subsequent L1A arrives exactly 2.9 μs later. At the test beam, this is monitored using test points on the CFEB boards and adjusted by changing the CCB L1A delay setting. This adjustment requires an operating CSC chamber and an external (e.g. scintillator) muon trigger.
- ALCT-TMB data transmission timing: data is multiplexed to 80 MHz in both directions between these boards. Two clock phases need adjustment for proper data transfer. The TMB supplies one main (transmit) clock for the ALCT board. To determine the proper phase of this clock, it is delayed in 1 ns steps using a PHOS4 delay ASIC chip (ref.) until ALCT output data is correctly latched at the TMB. In addition, some data is transferred from TMB to ALCT during normal operation, and in order that this data is received correctly at the ALCT a second (receive) clock phase is set using another PHOS4 delay chip channel. The TMB is read out through VME. This timing can be correctly adjusted without particles.
- CFEB comparator chip clock timing: the comparator chip clock on the CFEB is sent from the TMB. The phase of this clock determines whether the data is properly latched at the TMB. Fine timing to get optimal phase of this clock is adjusted by a scan across 25 PHOS4 delay settings. The quality of the timing is monitored by reading out the TMB through VME and counting the rate of 5-layer and 6-layer CLCT patterns. (A working CSC chamber and cosmic rays or test beam events are needed for this step).
- ALCT L1A delay setting: Once the ALCT is properly timed in, the ALCT L1A delay can be set. Events are taken at different L1A delay settings and the peak in ALCT efficiency is determined.
- TMB: L1A timed in (look at L1A window using internal logic scope and center by adjusting the window). Look at the "l1a_pulse_dsp" signal and make sure it is in the "l1a_window_dsp." Adjust the L1A pulse delay in VME address 74. Also look at the "alct_vpf_tp" pulse and make sure it is in the middle of the "clct_window_tp." Adjust the ALCT valid pattern pulse delay in VME address B2.
- Additional DMB timing: active FEB flags for ALCT and CLCT have to be timed in - direct signals on pins on DMB utility board (ugh!).
- Fine timing adjustment of ALCT delays: there is a fine delay setting for the ALCT board which delays the signal before latching. This is adjusted using test beam data until the efficiency for finding the ALCT pattern is maximized for a single time bin, as shown in Figure 6.

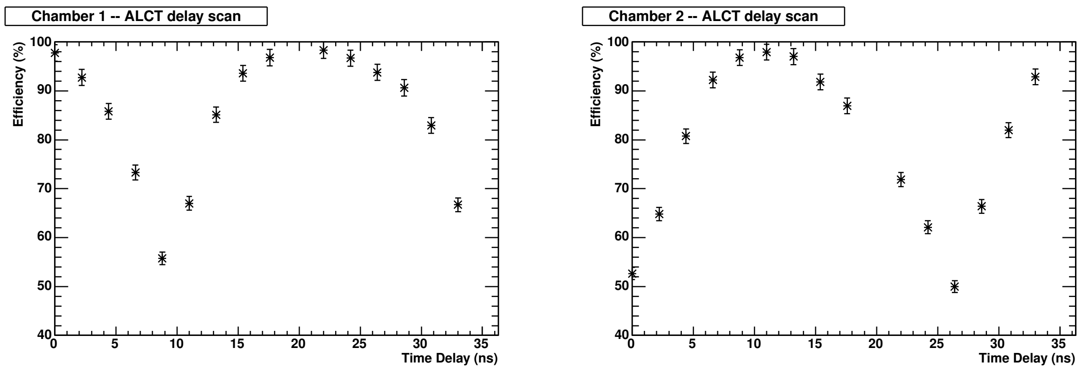

Figure 6: ALCT delay scans for chamber 1 (left) and chamber 2 (right). The efficiency for identifying the 'correct' bunch crossing is shown versus the ALCT fine delay setting. (Settings 0-15 are available in 2.2 ns steps.

***Describe checks of BX crossing numbers in various places, e.g. ALCT versus CLCT, TMB versus DMB, DMBs compared at DDU, both TMBs compared at Sector Processor input, and TMB/DMB/DDU checksums?

5 Results

5.1 Digital Comparison of Pattern-finding Simulation to LCTs

Raw hits, including time history, were recorded in the test beam data stream for both anode and cathode. These hits were fed into the official CMS Monte Carlo simulation of the ALCT-finding and CLCT-finding logic. Results of this digital simulation were compared bit-for-bit against the ALCT and CLCT patterns that were found. Initially, a large percentage of discrepancies were found, but this was traced to inaccuracies in the Monte Carlo simulation that were then fixed.

For ALCT pattern-finding, all but 0.0000x% agree. Disagreements were found in (what?).

For CLCT pattern-finding, all but 2.4% agree. Disagreements were found in those cases where trigger hits may have occurred before the start of the time history for them. Also, events were found containing two muon candidate tracks in which the second-best muon was recorded as the best, and vice versa. This appears to be a bug in the firmware and is being investigated... (*** update? ***)

5.2 Trigger Primitives Efficiency

*** Efficiency numbers for ALCT and CLCT finding: from logbook or from data runs?

*** High-rate pion test: include figures for ALCT rate versus pion rate and CLCT rate versus pion rate.

5.3 High Voltage and Threshold Scans

Varying the CSC chamber high-voltage (HV) setting changes the average pulse height by a factor of 2 for every 150 v change from nominal settings around 3600 v (***check this***). ALCT and CLCT efficiencies were studied as a function of HV. Additionally, the CLCT efficiency was studied versus raw hits threshold. These scans are shown in Figure 7.

5.4 Bunch Crossing Identification

Bunch crossing counters were reset by the TTC system after every orbit. After timing in, Figure 8 shows that there were 48 filled bunches out of each orbit 924 clocks long. The distribution of bunches with muons seen by the scintillator hodoscope (top) is entirely consistent with the distribution of muons as seen by the ALCT bunch identification logic.

Figure 8. The time of arrival of the muon, as seen by the cathode trigger, in clock ticks with respect to the ”LHC bunch 0”. Then BX efficiency:

Figure 9. Difference in time of the arrival of the muon (in 25 ns clock ticks) between the anode (ALCT) and cathode (CLCT) trigger circuitry and the timing from the scintillator hodoscope.

5.5 Trigger Primitives Position Resolution

5.5.1 Describe Stan's precision fitting algorithm

5.5.2 Single Chamber Results

-Reduced residuals of single chamber track fit are shown in Figure 9.

-The difference between the half -strip center and track fit positions are shown in Figure 9.

-Percentages of correct half-strip, +-1 half-strip, and +-2 or greater half-strips found by comparing the half-strip result to the track fit position: as a function of Qcluster. Figure 9.

-Percentages of correct half-strip, +-1 half-strip, and +-2 or greater half-strips found by comparing the half-strip result to the track fit position: as a function of chamber HV are shown in Figure 9.

-Percentages of correct half-strip, +-1 half-strip, and +-2 or greater half-strips found by comparing the half-strip result to the track fit position: as a function of track position within the strip. are shown in Figure 9.

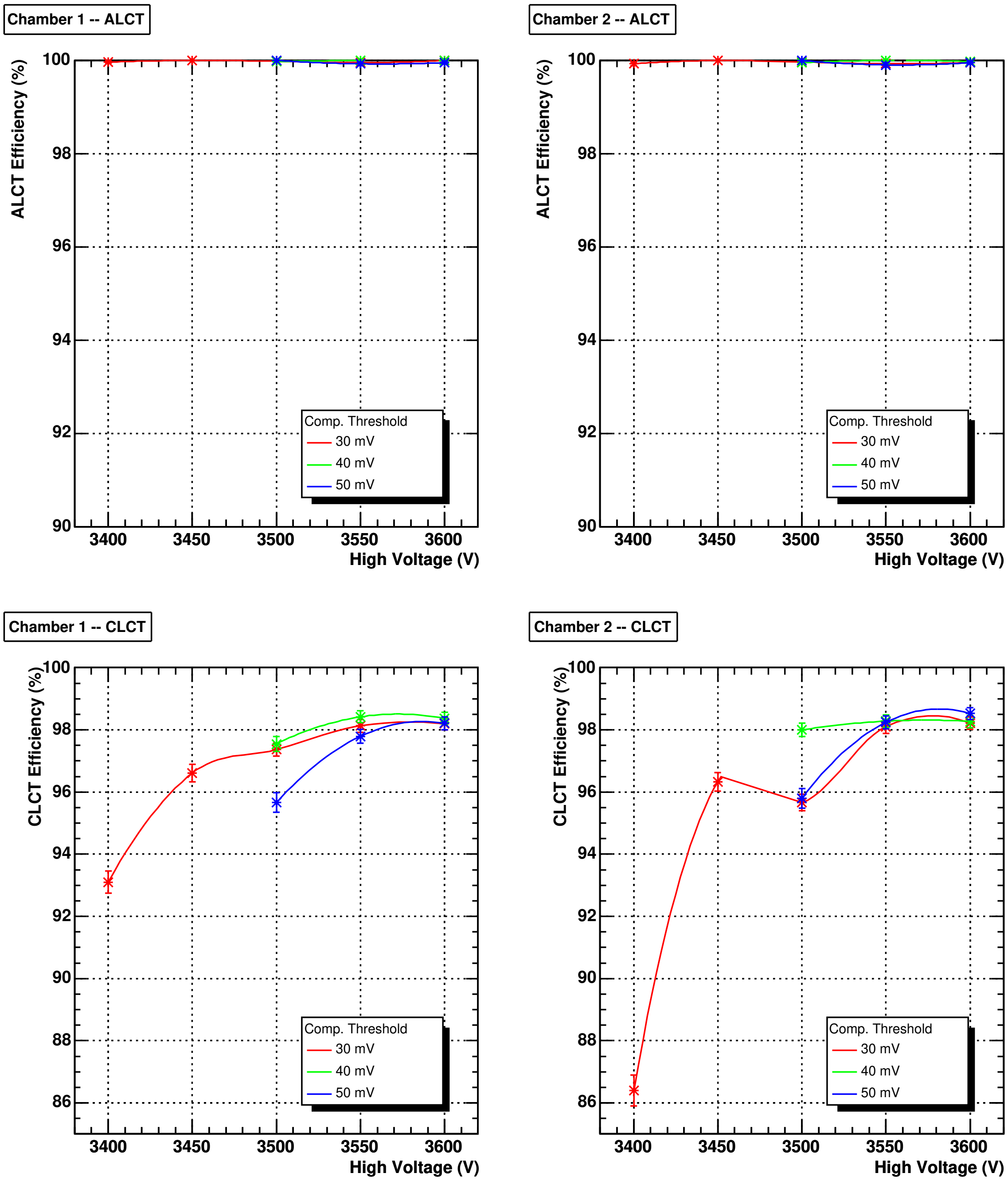

Figure 7: ALCT and CLCT efficiencies versus chamber high voltage.

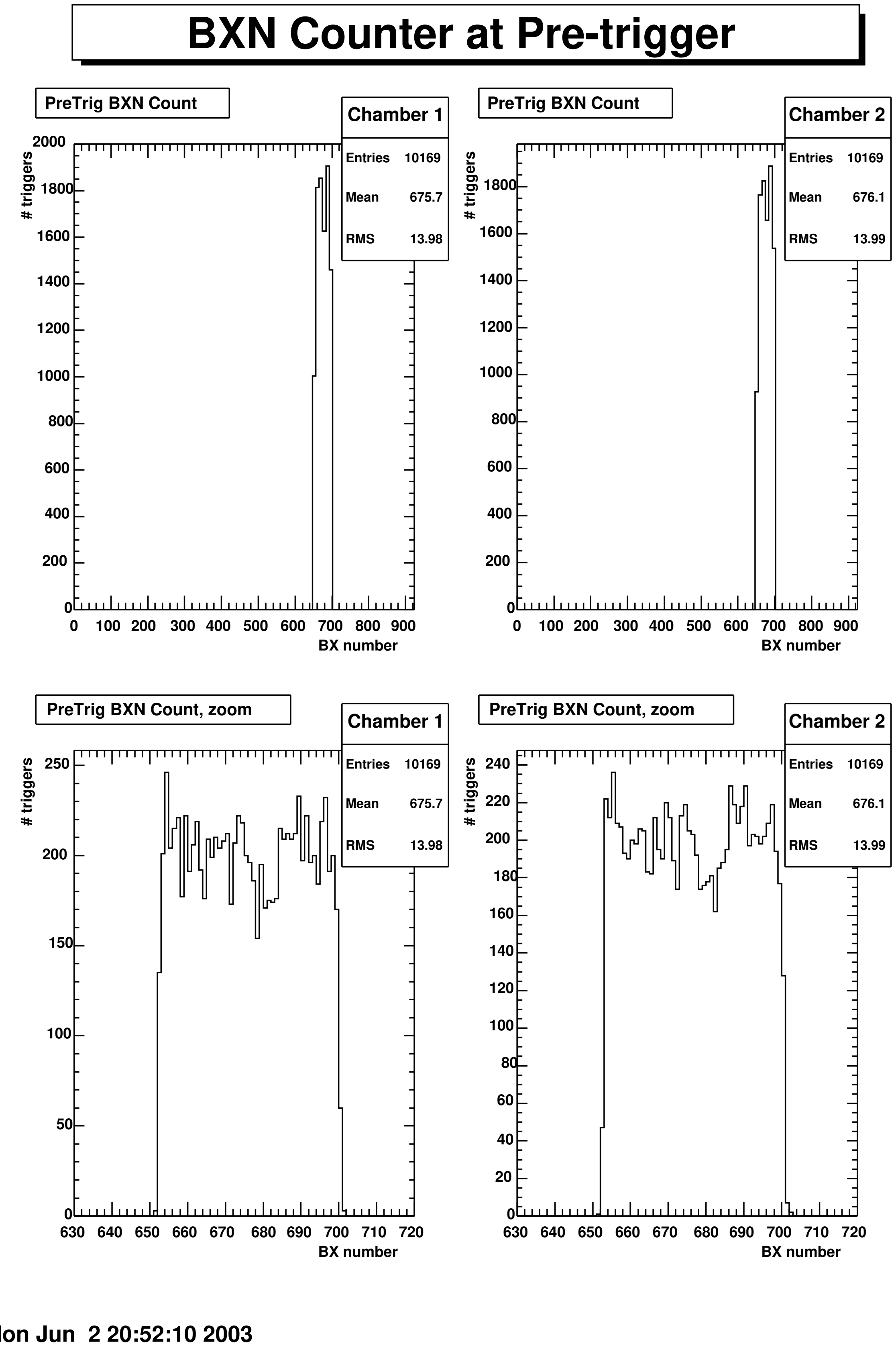

Figure 8: Bunch crossing with muon particles within the orbit containing 924 bunch crossings. On the top is shown the bunch crossings identified with the scintillator hodoscope. On the bottom is shown the bunch crossings as identified by the ALCT circuitry.

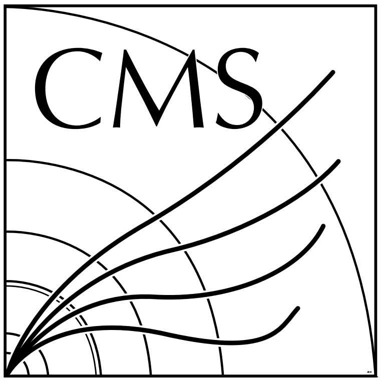

Figure 9: This is a placeholder for a future figure.

5.5.3 Two-chamber plots

Position of CLCT key half-strip numbers found in chamber 1 versus chamber 2 is shown in Figure 10. Both chambers were mounted with their midlines horizontal, but the area of the beam is slightly off-center. Nonetheless, there should be good correlation of position between the chambers. The data show that the CLCT positions found are well-correlated, although some small percentage of the events contain hits at large angles from 2nd muon tracks.

Presumably the angles of the muons don't vary as much as the vertical intercepts (since the chambers are much closer to each other than the distance from chamber 1 to the point of muon production). Therefore, the precision fitting code should be used to define an intercept, not a slope, which will have a large uncertainty since the path length within a chamber is only about 15 cm.

-Fit position in chamber 1 versus fit position in chamber 2. are shown in Figure 9.

-Difference between the fit positions in chambers 1 and 2. are shown in Figure 9.

-Difference between half-strip center in one chamber and track fit position in the other. are shown in Figure 9.

One could do this for the angle scans as well. Presumably when all the patterns are di-strip patterns, the resolution will be 4x worse or so. One can also look at the resolutions for half-strip versus di-strip patterns at the angles where there are both present. Since we dramatically preferred half-strip over di-strip patterns, this could give interesting insight into whether this was a good thing to do. ***

5.6 Chamber Angle Scans

Efficiencies to find CLCT half-strip and di-strip patterns versus chamber rotation angle ϕ_b are shown in Figure 11. The overall efficiency for finding any CLCT, which is the sum of half-strip and di-strip efficiencies, is also shown.

Chamber angle scans were done by tilting the chamber about a horizontal axis, which corresponds in CMS to varying the muon 'bend' angle (ϕ_b). During these scans, the polar angle (θ) of the chamber was held fixed at 20^o. Chamber qualities are defined as the number of layers with hits on the pattern minus three, i.e. a quality=3 pattern has the maximum possible six hits. Chamber patterns are ordered so that patterns 1 and 7 represent the extreme bend angles, while pattern 4 represents a straight-through pattern.

For chamber angles $\phi_b = 0^o$ (and $\phi_b = 10^o$), the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 12, with half-strip patterns shown on the left and di-strip patterns shown on the right. One sees that with the chamber at $\phi_b = 0^o$, i.e. vertical, nearly all of the events are found as straight-through half-strip patterns, with a majority being 6-hit patterns.

For chamber angles $\phi_b = -2.5^o$ and $\phi_b = +2.5^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 13, with half-strip patterns shown on the left and di-strip patterns shown on the right. At this angle, most of the events are found as half-strip patterns, but most are displaced from the straight-through central pattern.

For chamber angles $\phi_b = -5^o$ and $\phi_b = +5^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 14, with half-strip patterns shown on the left and di-strip patterns shown on the right.

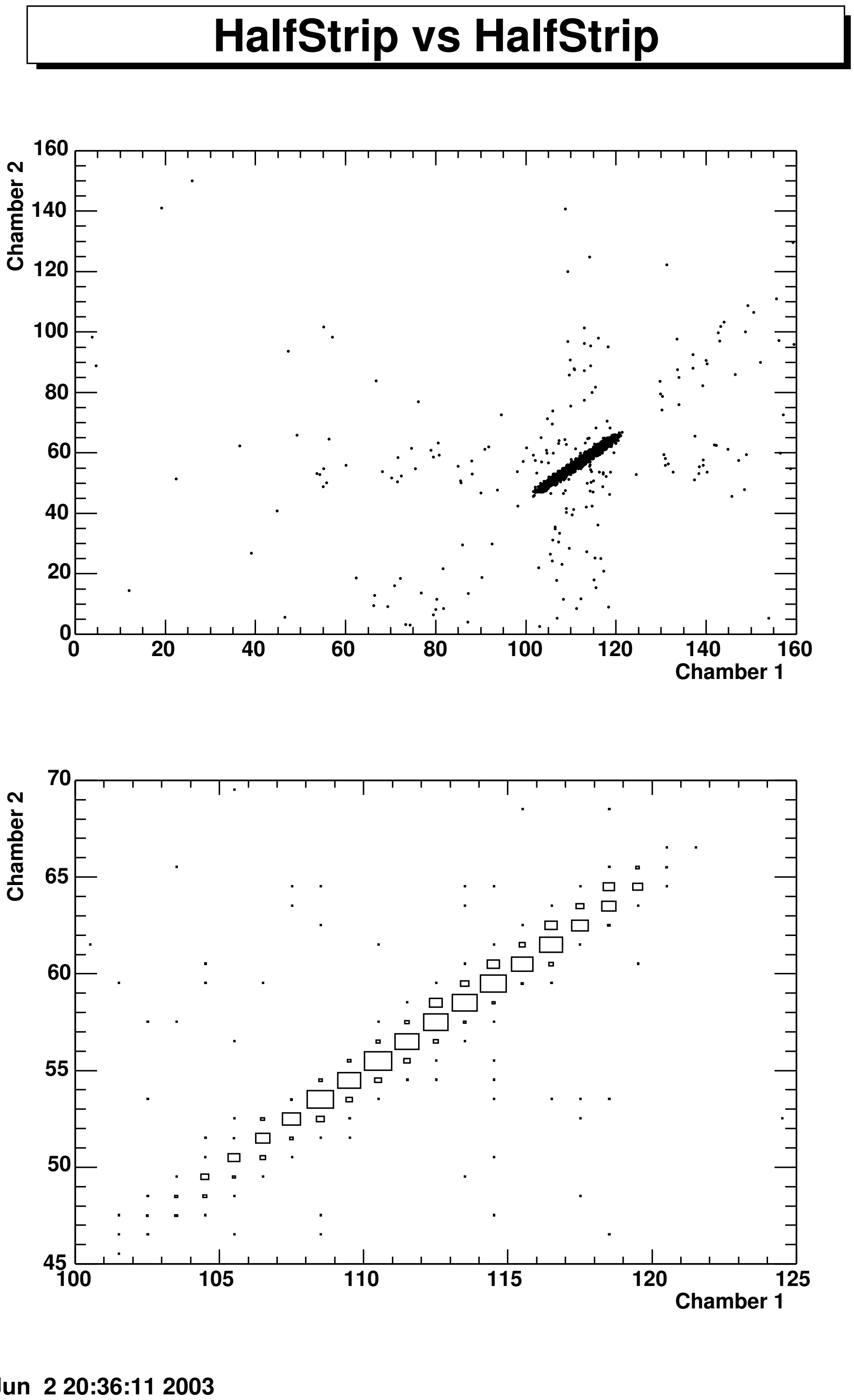

Figure 10: The CLCT 'key' half-strip found in the two chambers plotted against each other. The top plot shows all half-strips (0-159), while the bottom plot zooms in on the position where the beam is defined by the scintillator hodoscope.

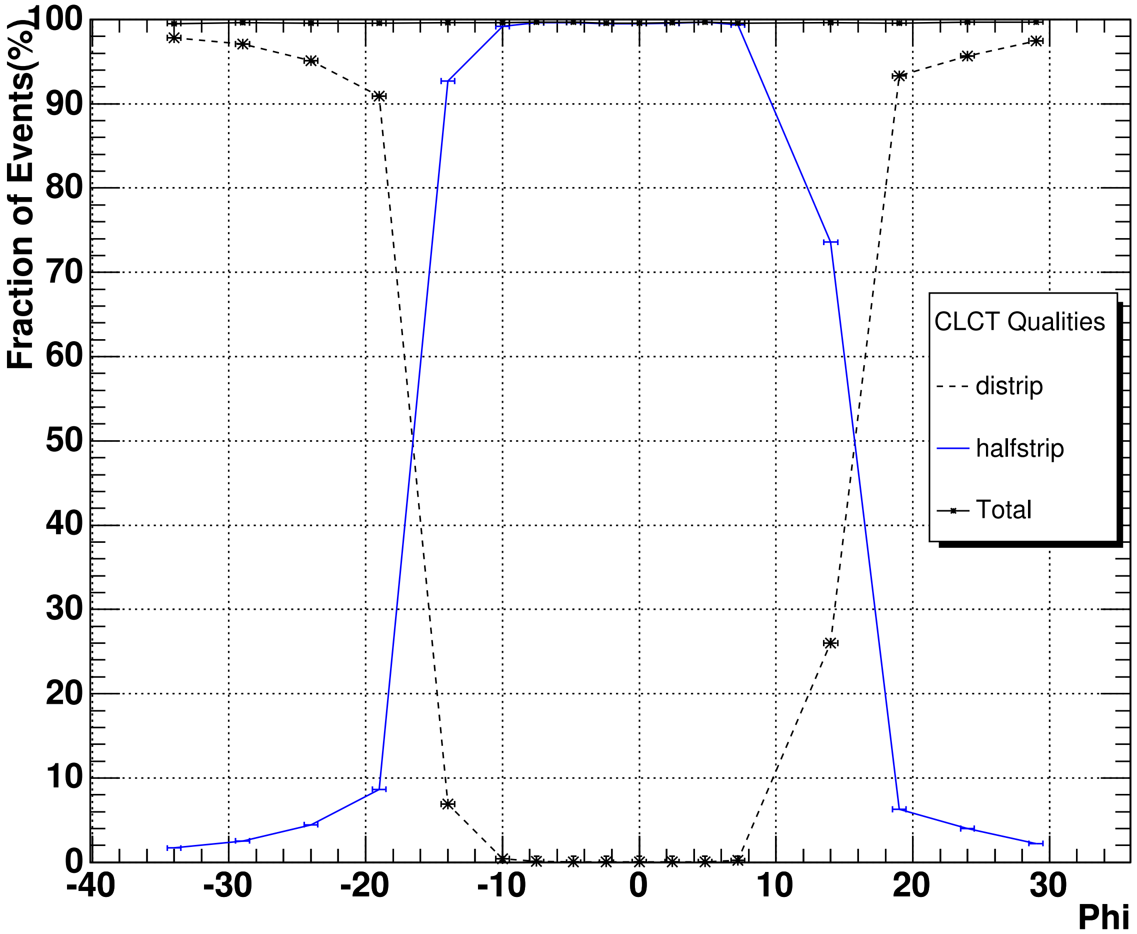

Figure 11: CLCT efficiency versus rotation angle ϕ_b.

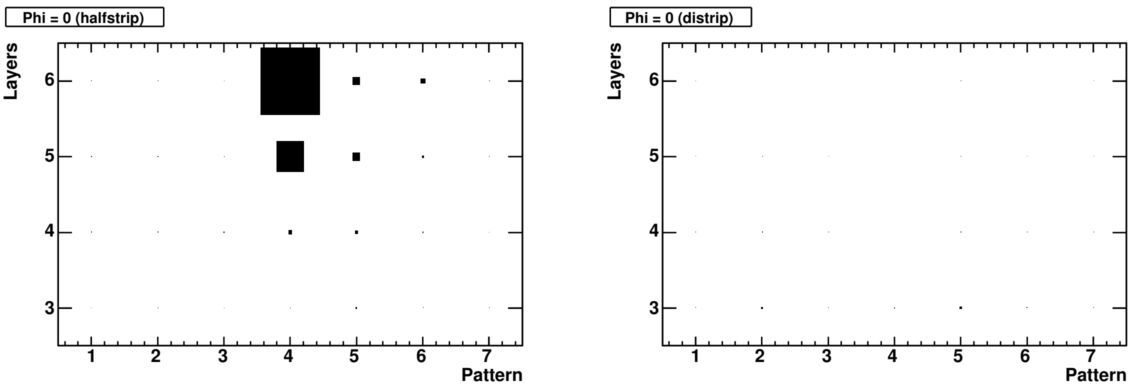

Figure 12: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angle $\phi_b = 0^o$.

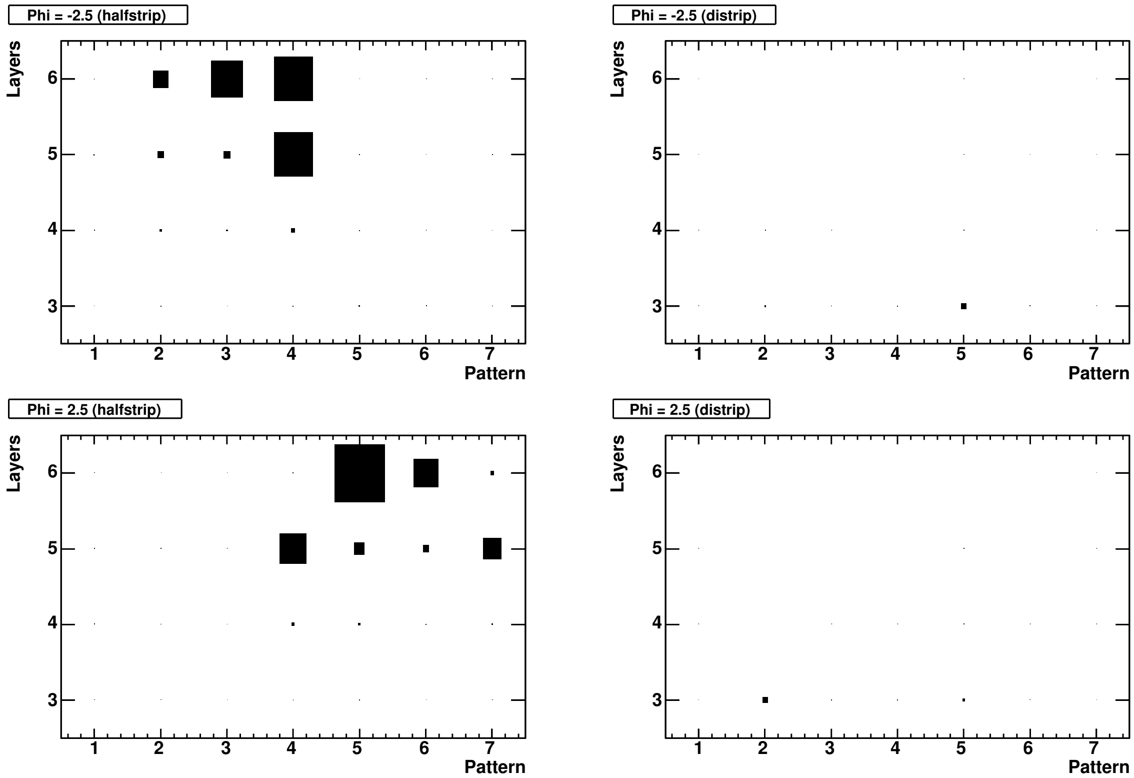

Figure 13: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -2.5^o$ (top) and $\phi_b = +2.5^o$ (bottom).

While the events are still found as half-strip patterns, these patterns have reached the edges of the fully half-strip acceptance (patterns 1 and 7).

For chamber angles $\phi_b = -7.5^o$ and $\phi_b = 7.5^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 15, with half-strip patterns shown on the left and di-strip patterns shown on the right. Again, the events are still found as half-strip patterns but at the edges of the fully half-strip acceptance (patterns 1 and 7).

For chamber angle $\phi_b = +10^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 16, with half-strip patterns shown on the left and di-strip patterns shown on the right. Angle $\phi_b = -10^0$ data was found to be corrupt (***or some such***).

*** What to say about this plot, for instance:? Again, the events are still found as half-strip patterns but at the edges of the fully half-strip acceptance (patterns 1 and 7). ***

For chamber angles $\phi_b = -15^o$ and $\phi_b = +15^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 17, with half-strip patterns shown on the left and di-strip patterns shown on the right. At these angles, the patterns are not fully within the half-strip envelope. Since the CLCT algorithm for choosing patterns prefers all half-strip patterns with two or more layers to all di-strip patterns having even 6 layers, the muon tracks are still found predominantly as half-strip patterns, but with much reduced quality, predominantly 2-hit or 3-hit patterns.

For chamber angles $\phi_b = -20^o$ and $\phi_b = +20^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 18, with half-strip patterns shown on the left and di-strip patterns shown on the right. At these angles, the muon tracks make patterns which is mostly beyond the half-strip acceptance with even two or three layers, and are found predominantly as di-strip patterns of high quality, although at the edge of the di-strip acceptance (patterns 1 and 7).

For chamber angles $\phi_b = -25^o$ and $\phi_b = +25^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 19, with half-strip patterns shown on the left and di-strip patterns shown on the right. At these angles, the muon tracks make patterns which are totally beyond the half-strip acceptance with even two or three layers, and are found almost always as di-strip patterns, although at the edge of the di-strip acceptance

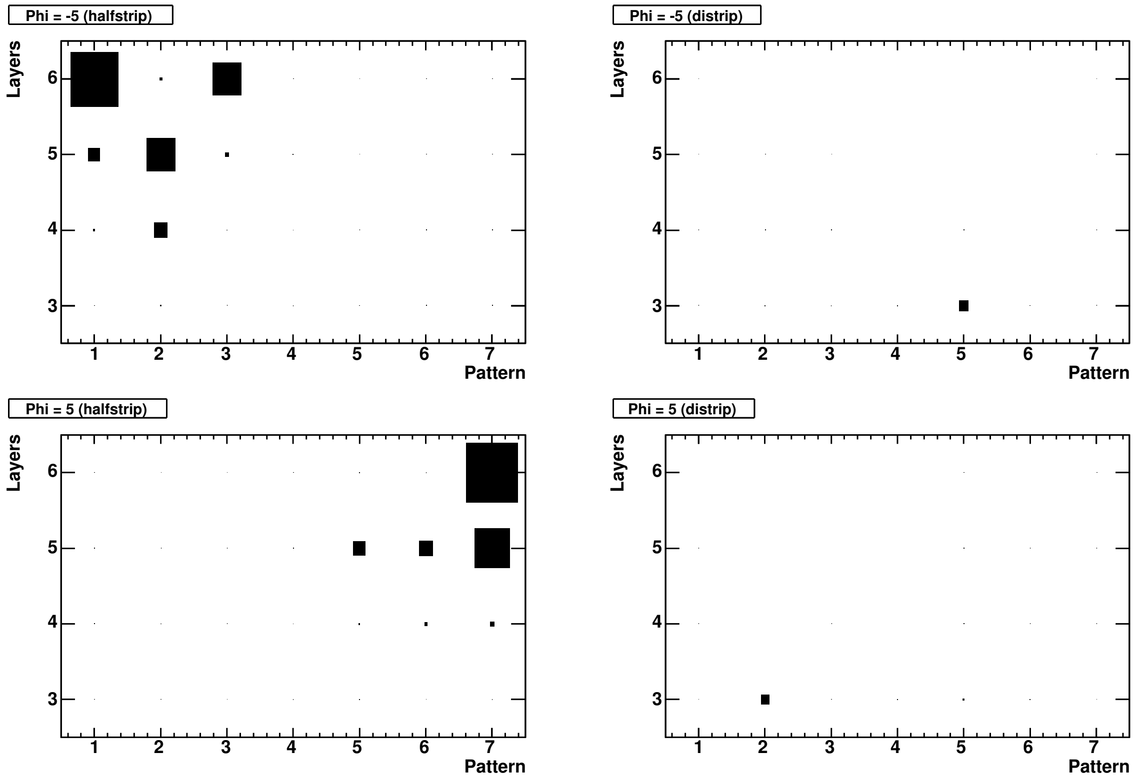

Figure 14: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -5^o$ (top) and $\phi_b = +5^o$ (bottom).

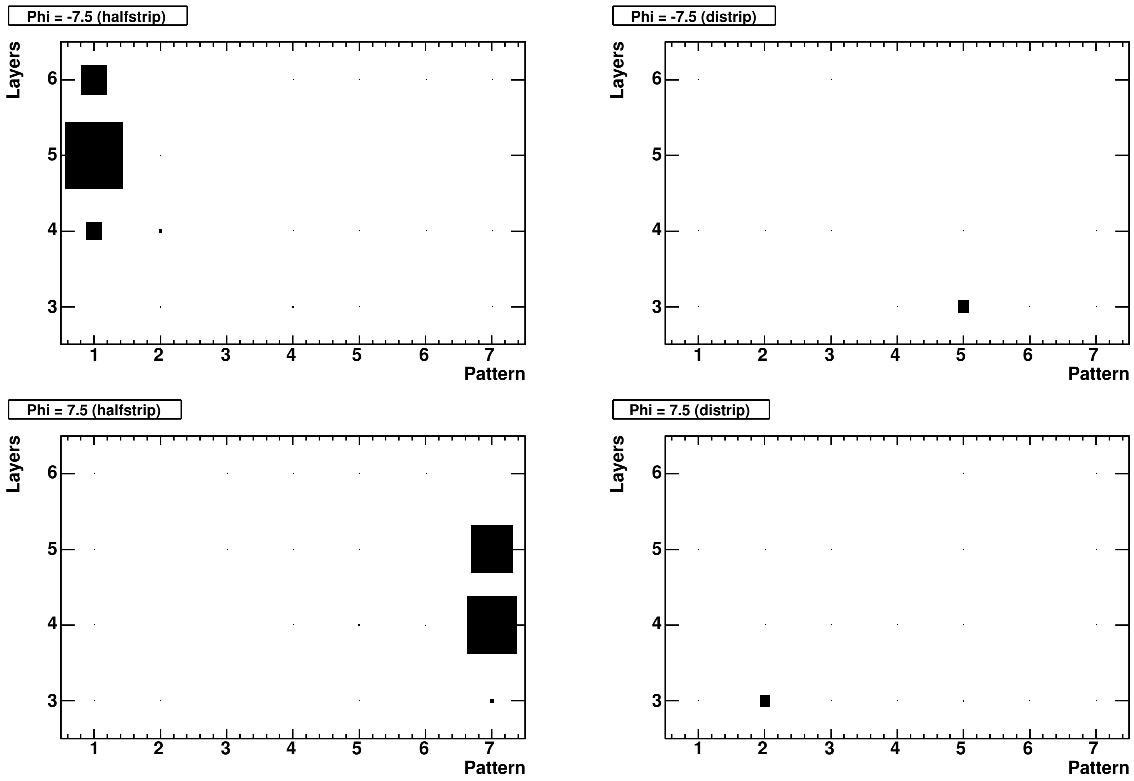

Figure 15: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -7.5^o$ (top) and $\phi_b = +7.5^o$ (bottom).

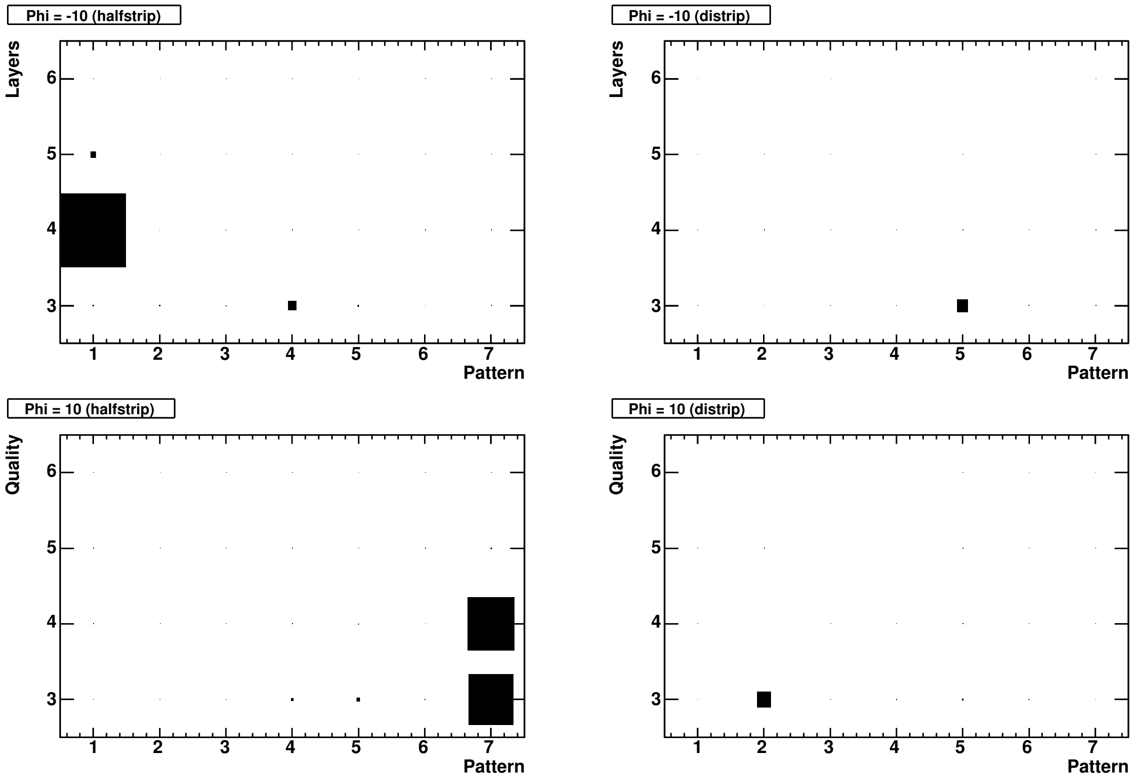

Figure 16: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angle $\phi_b = +10^o$ (bottom).

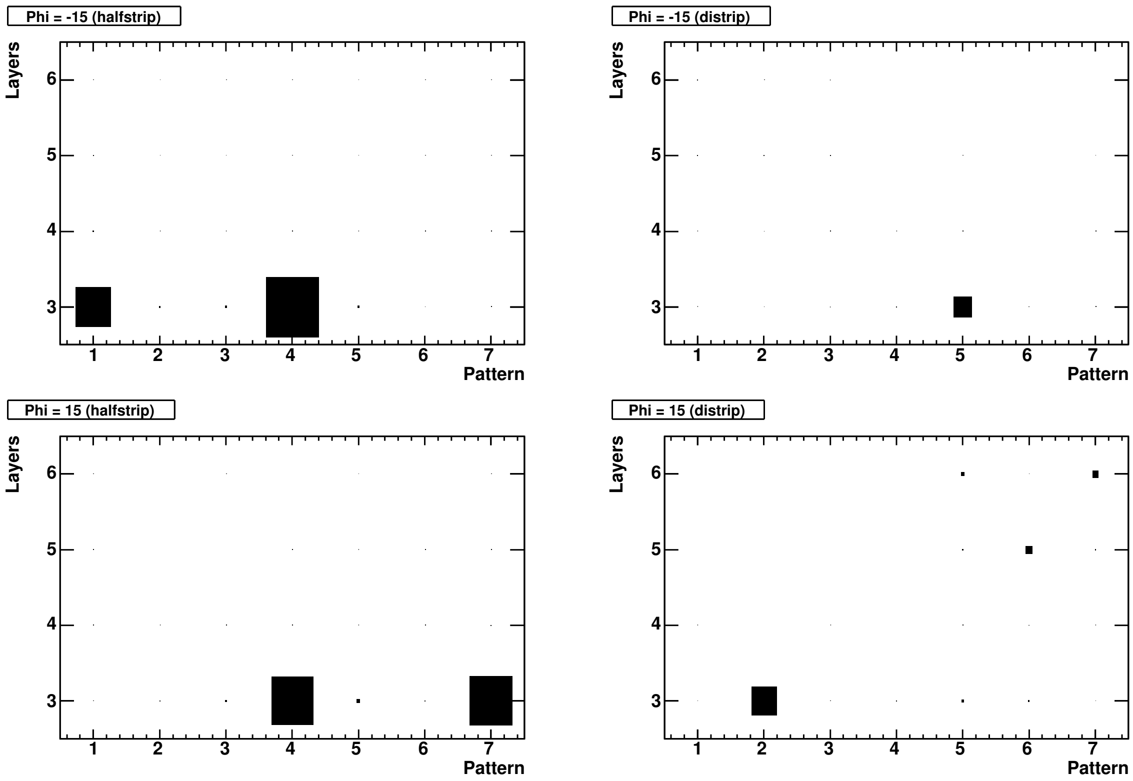

Figure 17: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -15^o$ (top) and $\phi_b = +15^o$ (bottom).

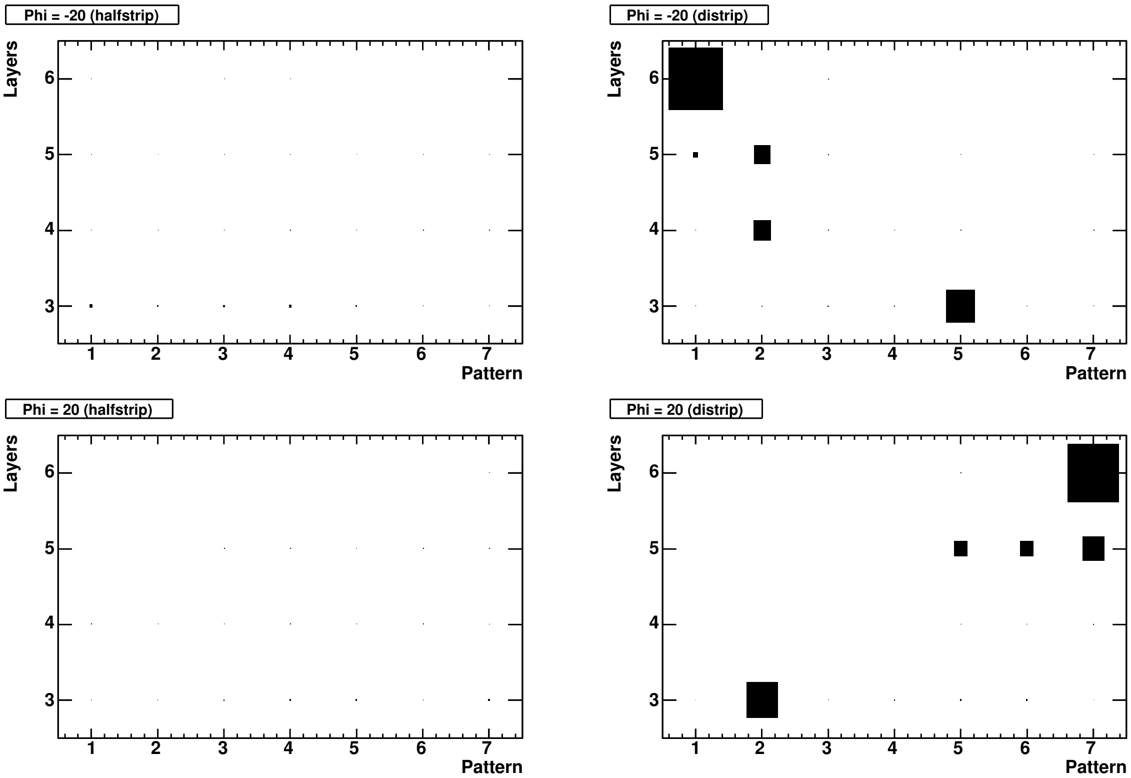

Figure 18: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -20^o$ (top) and $\phi_b = +20^o$ (bottom).

(patterns 1 and 7).

For chamber angles $\phi_b = -30^o$ and $\phi_b = +30^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 20, with half-strip patterns shown on the left and di-strip patterns shown on the right. At these angles, the muon tracks make patterns which are slightly beyond the di-strip acceptance. Therefore, the patterns found are at the edges of the di-strip pattern acceptance (patterns 1 and 7). The quality of these tracks is also somewhat degraded, with most patterns found as quality 2 (5-hit) patterns.

For a chamber angle $\phi_b = -35^o$ and $\phi_b = +35^o$, the distributions of qualities versus pattern numbers for the found patterns are shown in Figure 21, with half-strip patterns shown on the left and di-strip patterns shown on the right. At these angles, the muon tracks make patterns which are well beyond the di-strip acceptance. The patterns found are at the edges of the di-strip pattern acceptance (patterns 1 and 7), and the qualities are seriously degraded, with most patterns found as quality 1 (4-hit) patterns.

6 Conclusions

The peripheral crate electronics performed well at the summer 2003 test beam. Reliability was good, operations were handled remotely, and performance met expectations. Specifically:

- The efficiencies for finding trigger primitives were high. At rates much higher than seen at the LHC, the CLCT efficiency begins to drop.
- There was a range of HV operation over which the efficiencies were high.
- The position resolution was good.
- Cathode patterns and qualities varied with muon angle as expected.
- Further improvements are expected in the next generation

Some improvements can be forseen:

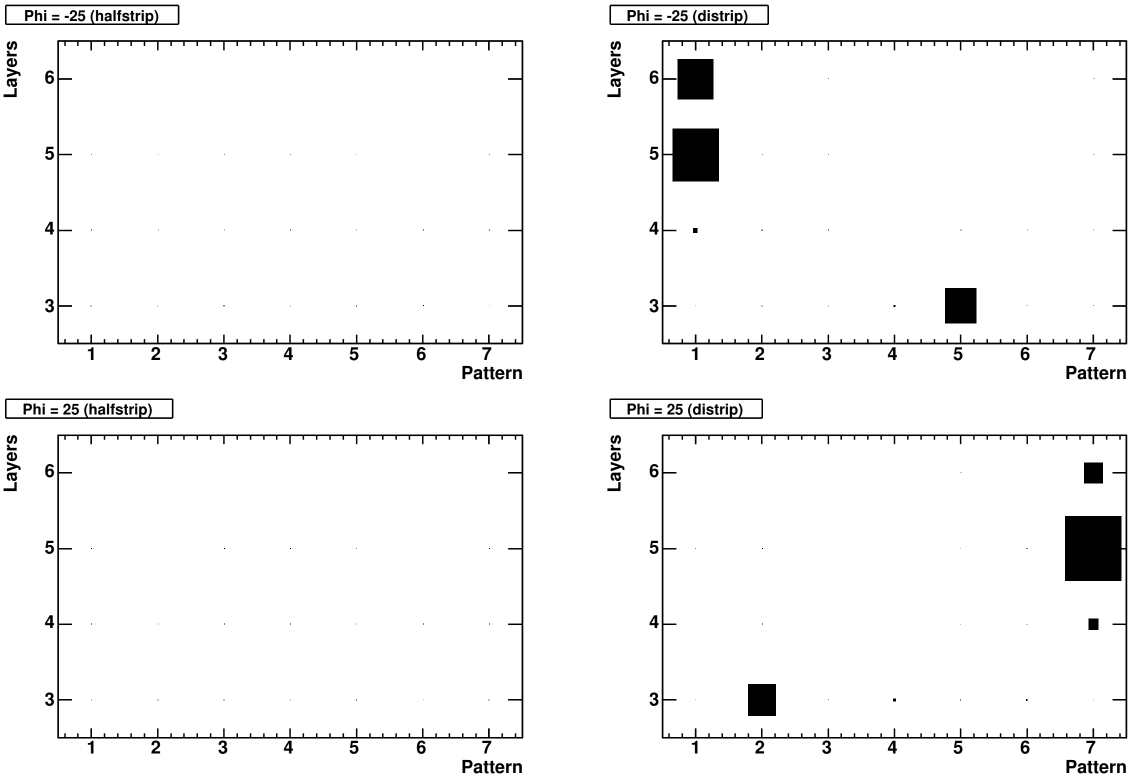

Figure 19: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -25^o$ (top) and $\phi_b = +25^o$ (bottom).

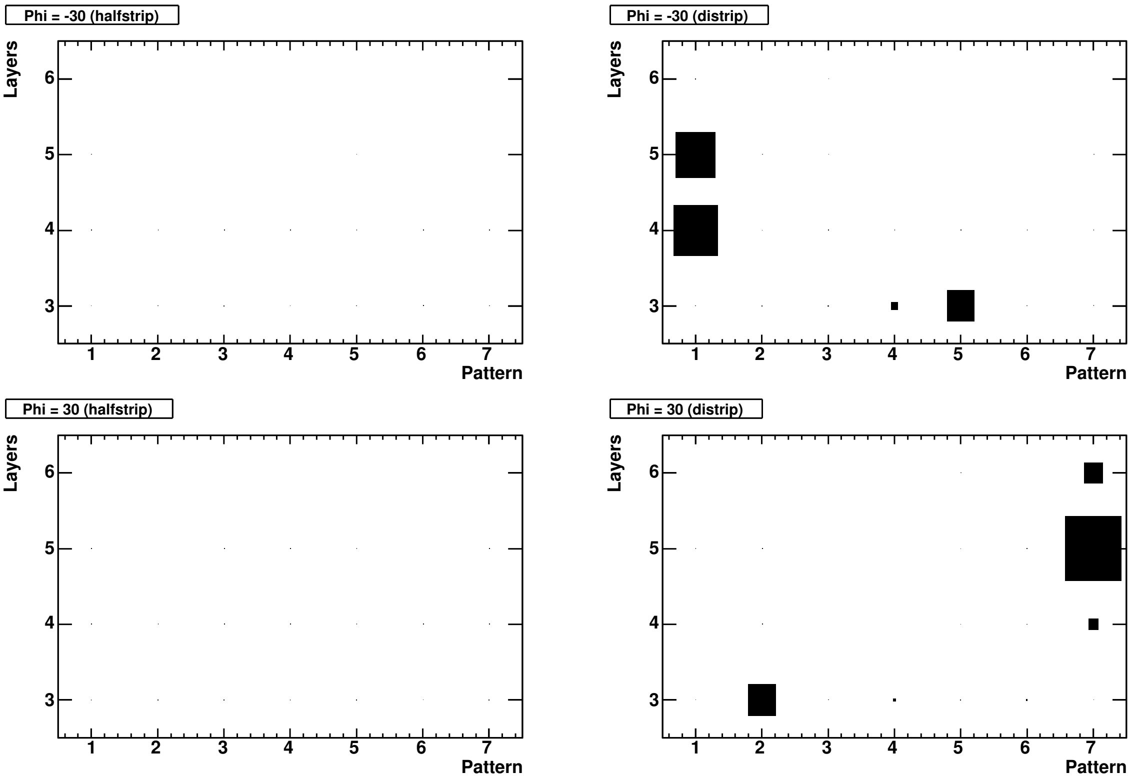

Figure 20: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -30^o$ (top) and $\phi_b = +30^o$ (bottom).

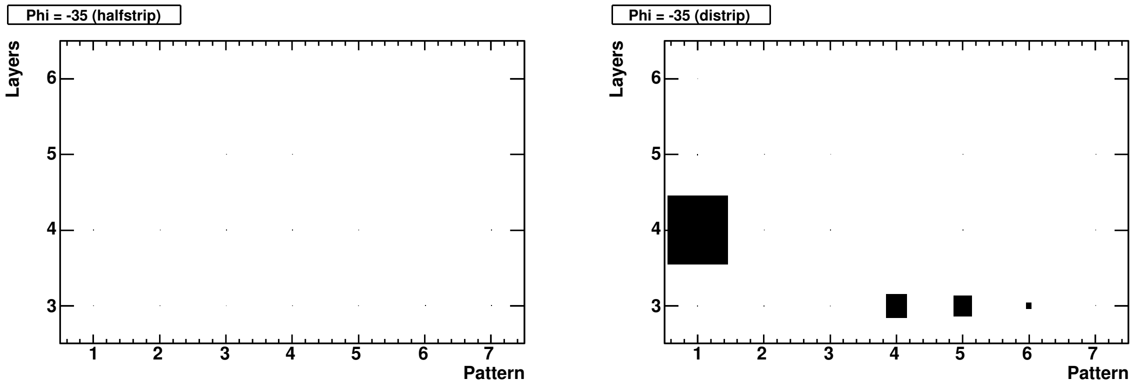

Figure 21: CLCT qualities versus pattern numbers, for half-strip patterns (left) and di-strip patterns (right), for rotation angles $\phi_b = -35^o$ (top) and $\phi_b = +35^o$ (bottom).

- The logic that orders the CLCT patterns preferred all half-strip patterns over all di-strip patterns. This was done in order to save space in the FPGA that performs the logic. In the next generation of TMB, a newer, larger FPGA allows us to order the patterns by a better algorithm.
- The ALCT produces 'ghosts', i.e. second muon stubs, in adjacent wire groups or in adjacent time bins. It is highly desirable to put in logic that removes such ghosts.

With these modest changes to the trigger hardware, the CSC trigger electronics used at the 2003 test beam will be ready to handle the job of muon triggering for the CMS detector at the LHC.

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